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EXAMINER	
TRAN, DENISE	

ART UNIT	PAPER NUMBER
2186	4

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,636	KRANTZ ET AL.	
	Examiner	Art Unit	
	Denise Tran	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2-3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-29 are presented for examination.

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract exceed 150 words in length. Correction is required. See MPEP § 608.01(b).

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 28, it is unclear whether "the controller" line 16 refers to "A disk drive controller" line 1 or "a buffer memory" line 4.

As per claim 29, it is unclear whether "the controller" lines 3-4 refer to "A disk drive controller" line 1 claim 28 or "a buffer memory" line 4, claim 28.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5, 8-11, 22, 24, and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proch et al., U. S. Patent No. 6,381,659 (hereinafter Proch) in view of Holmes, U.S. Patent No. 6,490,635 .

As per claims 1, Proch shows a buffer memory controller for a disk controller (e.g., fig. 2, el. 140) the buffer memory controller comprising:

A data buffer (e.g., fig. 2, fig. 2, buffer 144) configured to buffer write operation data between a buffer memory (e.g., fig. 2, buffer 25) and a write head of a disk (e.g., fig. 2, els 31-32);

A plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory (e.g., fig. 2, els. 152a-b, 154a-b, 148); and

Controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers (e.g., col. 6, lines

30-65). Proch does not explicitly show the use of a hard disk or a hard disk controller. Holmes shows the concept and the advantages of providing a hard disk or a hard disk controller (e.g., col. 1, line 15) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a hard disk or a hard disk controller because it would allow more data to be stored and accessed more quickly.

As per claims 2-3 and 25-27, Proch shows a plurality of blocks count registers configured to stored, for each of the write operations, the corresponding amount of write operation data stored within the buffer memory (e.g., col. 8, lines 25-45); wherein the controller logic is configured to perform the transfers based additionally upon the quantities stored in the block count registers (e.g., col. 9, lines 25-45); and Proch teaches for each of write operations, loading a different one of a plurality of block count registers of the buffer memory controller with a value specifying an amount of write operation data associated with the respective write operation (e.g., col. 7, lines 40-55; col. 8, lines 25-45); wherein the address registers and the block count registers are load with the addresses and amounts of the data of the write operations in the order in which the write operations are to be executed (e.g., col. 7, lines 40-55; col. 8, lines 25-45).

As per claims 5, 8-11 Proch shows the data buffer operated as a FIFO (e.g., fig. 2, FIFO 144); the controller logic is further configured to transfer the data of at least two operations based upon a single command to the buffer memory controller (e.g., col. 10 , lines 60); a busy flag to indicate whether the address registers are full (e.g., fig. 3b,

FIFO full); the number of address registers is at least 4, (e.g., fig. 2, els. 152a-b and 154a-b) or at least 8 (e.g., col. 11, lines 15-20).

As per claims 22 and 24, Proch shows a method of operating a disk controller , the method comprising:

Loading a first address register of a buffer memory controller with an address in a buffer memory of write operation data of a first write operation (e.g., col. 6, lines 50-65); and

Loading a second address register of a buffer memory controller with an address in the buffer memory of write operation data of a second write operation (e.g., col. 6, lines 50-65);

Wherein the first address register is different than the second address register, wherein the first address register is different than the second address register, and wherein the first write operation is different than the second write operation (e.g., col. 10, line 45 to col. 11, line 15); or receiving a command to provide the write operation data of the plurality of write operations (e.g., col. 10 , lines 60). Proch does not explicitly show the use of a hard disk or a hard disk controller. Holmes shows the concept and the advantages of providing a hard disk or a hard disk controller (e.g., col. 1, line 15) are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a hard disk or a hard disk controller because it would allow more data to be stored and accessed more quickly.

As per claim 28, Proch shows a disk drive controller comprising:

a buffer memory for storing write operation data (e.g., fig. 2, el. 25);

a buffer memory controller comprising:

A data buffer (e.g., fig. 2, fig. 2, buffer 144) configured to buffer write operation data between a buffer memory (e.g., fig. 2, buffer 25) and a write head of a disk (e.g., fig. 2, els 31-32);

A plurality of address registers configured to store, for each of a plurality of write operations, an address identifying a location of corresponding write operation data stored within the buffer memory (e.g., fig. 2, els. 152a-b, 154a-b, 148); and

Controller logic configured to transfer, for each of the write operations, the corresponding write operation data from the buffer memory to the data buffer based at least upon the corresponding address stored in the address registers (e.g., col. 6, lines 30-65). Proch does not explicitly show firmware code that is executed by a microprocessor, the firmware code configured to enable the microprocessor perform write operations in an order other than the other in which the write operations are received by the controller. Holmes firmware code that is executed by a microprocessor, the firmware code configured to enable the microprocessor perform write operations in an order other than the other in which the write operations are received by the controller (e.g., col. 1, lines 20-25 and lines 35-60; and col. 5, lines 60-64. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching Holmes into the system of Proch because it would allow enhance disk drive performance.

7. Claims 4, 6-7, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proch et al., U. S. Patent No. 6,381,659 (hereinafter Proch) in view of Holmes, U.S. Patent No. 6,490,635, with respect to claims 1, 22 , and 24, and further in view of Official Notice.

As per claims 4 and 6-7, Proch does not explicitly show the block count registers operate as a FIFO, data register is configured to supply write operation data to a disk formatter; or the address registers operate as a FIFO. "Official Notice" is taken that both the concept and the advantages of providing a block count registers as FIFO, disk formatter, or address registers as FIFO are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide providing a block count registers as FIFO, providing data to a disk formatter, or address registers as FIFO because it would allow address or block count to be access in the same order as received and data to be processed in a predetermined format.

As per claim 23, Proch shows the controller logic is further configured to transfer the data of at least two operations based upon a single command to the buffer memory controller (e.g., col. 10 , lines 60). Proch does not explicitly show providing the write operation data of the plurality of write operations to a disk formatter. "Official Notice" is taken that both the concept and the advantages of providing data to a disk formatter are well known and expected in the art. It would have been obvious to one of ordinary skill

in the art at the time the invention was made to provide providing data to a disk formatter because it would allow data to be processed in a predetermined format.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 12 ,18- 20,22, and 24-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Holmes, U.S. patent No. 6,490,635.

As per claim 12, Holmes teaches a method of operating a hard disk unit, the method comprising:

(A) receiving a first write operation (e.g., col. 2, lines 19-20);

(B) subsequent to (A), receiving a second write operation (e.g., col. 2, lines 19-20);

(C) writing the data of the second write operation to a disk (e.g., col. 1, lines 15-25 and lines 40-60; and col. 5, lines 61-64).

As per claim 18, Holmes shows a method comprising:

receiving a plurality of write operations (e.g., fig. 3A, els. 312, 320); and for each of the write operations, loading a different one of a plurality address registers (i.e., Ram

, memory unit is a collection of storage registers; e.g., fig. 5, els. LBA and col. 3, lines 15-35) of a buffer memory controller (e.g., fig. 4, el. 400 or el. 500) with an address within a buffer memory write operation data of the respective write operation (e.g., col. 5, lines 10-12).

As per claims 22 and 24, Holmes shows a method of operating a disk controller , the method comprising:

Loading a first address register of a buffer memory controller with an address in a buffer memory of write operation data of a first write operation (i.e., Ram , memory unit is a collection of storage registers; e.g., fig. 5, els. LBA and col. 3, lines 15-35; col. 5, lines 10-12); and

Loading a second address register of a buffer memory controller with an address in the buffer memory of write operation data of a second write operation (i.e., Ram , memory unit is a collection of storage registers; e.g., fig. 5, els. LBA and col. 3, lines 15-35; col. 5, lines 10-12);

Wherein the first address register is different than the second address register, wherein the first address register is different than the second address register, and wherein the first write operation is different than the second write operation (i.e., Ram , memory unit is a collection of storage registers; e.g., fig. 5, els. LBA and col. 3, lines 15-35; col. 5, lines 10-12); or receiving a command to provide the write operation data of the plurality of write operations (e.g., col. 5 , lines 30-35).

As per claims 19-20 and 25-27, Holmes teaches for each of write operations, loading a different one of a plurality of block count registers of the buffer memory controller with a value specifying an amount of write operation data associated with the respective write operation (i.e., Ram , memory unit is a collection of storage registers; e.g., fig. 5, els. block count 540 and col. 3, lines 15-35); wherein the address registers and the block count registers are load with the addresses and amounts of the data of the write operations in the order in which the write operations are to be executed (e.g., col. 5, lines 63-67); for one of the write operations, transferring write operation data from the buffer memory, the amount of which write operation data is specified by the value in the corresponding block count register and the address of which write operation data is specified by the address corresponding address register (e.g., col. 3, lines 15-35); repeating (D) for each of the remaining write operations (e.g., col. 3, lines 15-35).

10. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Holmes, U.S. Patent No. 6,490,635 in view of Official notice with respect to claim 12 .

As per claim 21, Holmes does not explicitly show providing the write operation data of the plurality of write operations to a disk formatter. "Official Notice" is taken that both the concept and the advantages of providing data to a disk formatter are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide providing data to a disk formatter because it would allow data to be processed in a predetermined format.

11. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holmes, U.S. Patent No. 6,490,635 in view of Au, U.S. Patent No. 5,729,718, with respect to claim 12 .

As per claims 13-17, Holmes does not explicitly show the use of determining that the first write operation and the second write operation write data to the same track; determining that second write operation has a lower ending sector number than the starting sector number of the first write operation; determining that second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track; wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution; wherein a portion of the data of the first write operation and the data of the second write operation are written to the disk during a single revolution. Au shows determining that the first write operation and the second write operation write data to the same track (e.g., col. 4, lines 35-40); determining that second write operation has a lower ending sector number than the starting sector number of the first write operation (e.g., (e.g., col. 3, 50-55); determining that second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track; wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution; wherein a portion of the data of the first write operation and the data of the second write operation are written to the disk during

a single revolution. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Au to the system of Holmes because it would allow improve data throughput of a storage device by reordering commands to minimize latency including both seeking time and rotational latency.

As per claims 14-17, Holmes shows determining that second write operation has a lower ending sector number than the starting sector number of the first write operation (e.g., col. 6, lines 45-65; col. 6, lines 25-30; col. 5, lines 40-55); determining that second write operation is located before the first write operation relative to the position where the write head of the disk is capable of first writing to the track (e.g., col. 6, lines 25-30; col. 5, lines 40-55); wherein a portion of the data of the first write operation and a portion of the data of the second write operation are written to the disk during a single revolution (col. 4, lines 35-58); wherein a portion of the data of the first write operation and the data of the second write operation are written to the disk during a single revolution (col. 4, lines 35-65).

12. Claim 29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Megiddo (6574676) is cited to show scheduling commands by total access time.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Denise Tran

D.T.
November 6, 2003